SPECIFICATION

Please amend paragraph [0018] as shown below to correct a typographical error. No new matter is added.

[0018] FIG. 5 illustrates a four-bundle cluster processor architecture 300 suitable for use with the invention. Architecture 300 includes two processing cores 302A and 302B. Each core 302 includes an associated register file 304 and pipeline execution units 306, as shown. Execution units 306 include internal bypassing capability, as indicated by arrows 308A, 308B. Cores 302A, 302B may be identical. Units 306A, 306B write-back to register file 304 by control lines 310A, 310B, respectively. If required, data transfer between cores 302 may occur via multiplexers 312A, 312B, as shown; a latch 314 may be used to couple data from one core 302 to the execution units 306 of the other core. Data from one core 302 that is architected to the register file ~~204~~ 304 of the other core may be written, as shown, through a latch 316.